24.4 A 4-Channel 3.1/10.3Gb/s Transceiver Macro with a Pattern-Tolerant Adaptive Equalizer

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In multi-gigabit/s chip-to-chip communication, an adaptive equalizer is often used to automatically compensate for frequency-dependent loss such as skin effect and dielectric loss. Previous adaptive equalizers assume particular, e.g., random, data patterns [1], and may fail to work for unexpected data patterns. Although data-aided adaptive schemes [2,3] that use the slicer output as the reference may improve tolerance for data-pattern variation, they cannot completely solve the problem, because equalizer parameters may drift to totally bad values for the worst cases such as single-frequency periodic patterns. On the other hand, such periodic data patterns are not necessarily rare unless data is scrambled, because real data is heavily correlated rather than random. Consequently, conventional adaptive schemes used in non-scrambled interfaces such as 10GBASE-CX4 may drift when running continuously, or suffer from compromised performance when fixed to a static state based on initial tuning. A 4-channel 3.1/10.3Gb/s transceiver macro with a pattern-tolerant adaptive equalizer has been developed for a 10Gb Ethernet switch chip. Each macro is configurable as 4 channels of 3.125Gb/s (3G mode), or 1 channel of 10.3125Gb/s with a 161MHz reference clock driver for an optical module (10G mode).

Figure 24.4.1 shows the block diagram of the receiver. The equalizer (EQ) output is sampled by 2 sets of 2-way interleaved decision circuits that produce 2 data values and 2 boundary values in turn. Here, the data values are sampled at the center of the eye and the boundary values are at transitions. After de-multiplexing, the data and boundary values are used for phase detection in the CDR loop [4] as well as for the EQ gain and offset controls [3]. The EQ is a digitally controlled analog derivative EQ as shown in Fig. 24.4.2. Attenuated high-frequency components are boosted by the derivative path [5]. Since amplitude information is not available, either the DC or the derivative path is always set to maximum gain. In the following, the EQ gain refers to boosting of the high-frequency components, which is implemented either by increasing derivative-path gain or decreasing DC-path gain.
A previous ISI-detection scheme using a boundary value was based on the pulse width [3]. In the present work, the ISI level is generally defined as the inverse of correlation between the boundary value and the data value 1.5UI preceding the boundary, as shown in Fig. 24.4.3. If an ISI level is -1 (or +1), the EQ gain may be too low (or too high). If data is random, ISI levels at all transitions may be used to adjust EQ gain, because unpredictable boundary values such as for 0101 sequence are statistically cancelled out.

On the other hand, in order to obtain consistent results for non-random data, the pattern-balancing adaptive scheme shown in Fig. 24.4.4(a) uses the ISI level only when a particular data sequence called a filter pattern (FP) is received. Randomly cycling through a set of FPs ensures balance between data sequences. When the initial FP is received, EQ gain is updated according to the ISI level, and a next FP is randomly selected. As long as the selected FP is missing in the incoming data, the adaptive control is inhibited and holds the current EQ gain. No time-out is implemented. This is a deliberate and beneficial design feature, as it prevents the EQ from drifting when it encounters single-frequency periodic patterns. The adaptive control resumes when it encounters the current FP, adjusting EQ gain and selecting the next FP. If incoming data is mostly periodic with sparse random data, the adaptive control works slowly but steadily using only the limited random data. The whole set of FPs is chosen from only those patterns observed in the startup and idle periods so that the adaptive control never stops during such periods. During start-up, EQ gain starts from a low value, because the ISI level may be false negative for extremely over-compensated low-loss channels. Other than that, nothing special such as training sequence is required. The penalty of the scheme is low loop bandwidth for random patterns, because only one out of 16 transition patterns is watched at a time.

In addition, as shown in Fig. 24.4.4(b), the adaptive EQ control also uses random-phase down-sampling that saves power without degrading the tolerance for middle-frequency jitter and periodic patterns synchronous to the down-sampling cycle – a drawback of conventional fixed-phase down-sampling.

The transmitter is an LVDS-type driver, a bridge-switched differential current-source driver [6] with 5 programmable fingers to differentiate swing between 3G and 10G modes and to form an FIR HPF for pre-emphasis or an FIR LPF for slew-rate control as the reference clock driver.

Figure 24.4.5 shows the evaluation results for the pattern tolerance of the adaptive scheme. The horizontal axis represents the gain of the equalized channel at $f_s/2$ relative to $f_s/16$ in dB. The vertical axis represents the average ISI level measured for a mostly periodic data pattern. In this measurement, the EQ gain is fixed for characterization. If the adaptive control is enabled, the EQ gain will go up or down with a small loop constant for each sample of ISI level so that it will converge where the average ISI level crosses zero with a positive slope. If the average ISI level is always positive, it will converge to the left end. If the average ISI level crosses zero with a negative slope, it will be meta-stable. The measurement is repeated for 256 data patterns that cover all possible 8B10B encoded Ethernet frames filled with a fixed data byte. The frame length is max (3770b), and the header (30b) is randomized. BER (measured for $>10^{-12}$ or estimated from bathtub curve) for PRBS31 is also shown for reference. The top plots show the average ISI level for all transitions. It corresponds to a conventional adaptive scheme that assumes a random data pattern. For many data patterns, it converges to some point, although its variation is very large. There are several pathological patterns, containing only low- or high-frequency components in the data payload, for which the characteristics are totally different from others, suggesting that the adaptive control will drift for those patterns. The bottom plots show the average ISI level measured with pattern balancing. It is calculated from the ISI level only when the FP is received. The variation of the adaptive control for data-pattern variation is from -1.7 to 2.2dB in terms of the equalized channel gain at $f_s/2$ relative to $f_s/16$.

Figure 24.4.6 shows the die micrograph. The macro includes 4 TX channels, 4 RX channels, and 1 clock unit. The macro area is $3.52mm^2$ using a 90nm CMOS technology.

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[6] *IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI), 1596.3 SCI-LVDS Standard,* IEEE Std 1596.3-1996, 1996.

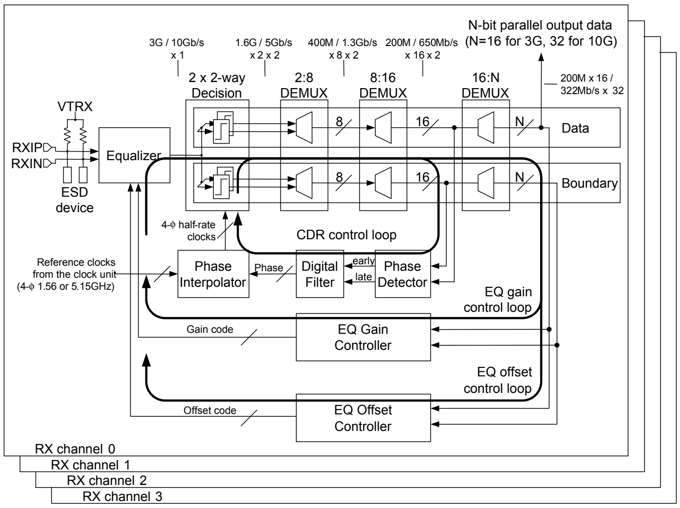


Figure 24.4.1: Receiver block diagram.

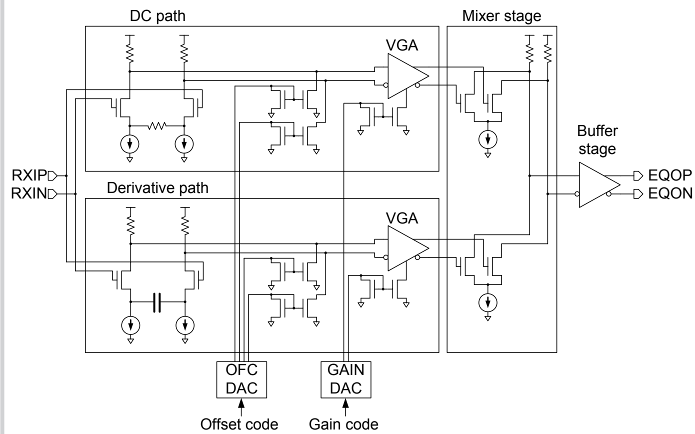
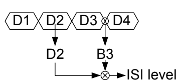


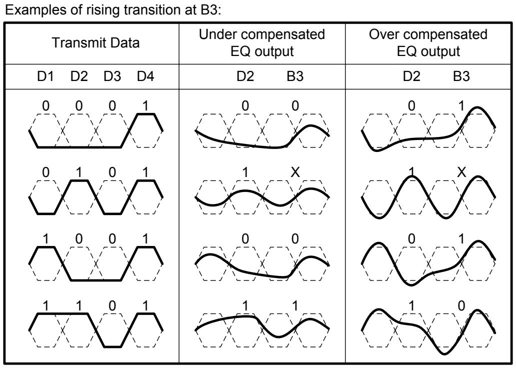
Figure 24.4.2: Equalizer circuit.



ISI detection

D1	D3 D4	D2	B3	ISI level	Interpretation	EQ gain
X	rise (0 1) or fall (1 0)	0	0	-1	Under compensated	Too low
		0	1	+1	Over compensated	Too high
		1	0	+1	Over compensated	Too high
		1	1	-1	Under compensated	Too low

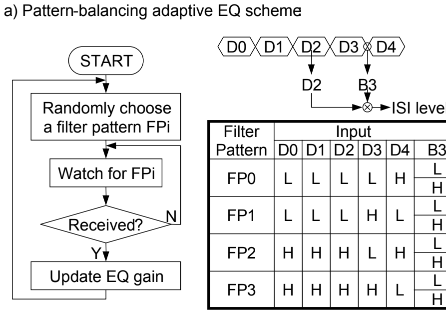
Examples of rising transition at B3:



X: Depends on data before D1.
If data is random, it is statistically cancelled.

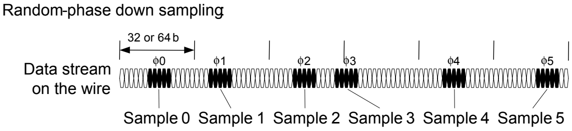
Figure 24.4.3: ISI-level detection using the boundary value.

a) Pattern-balancing adaptive EQ scheme



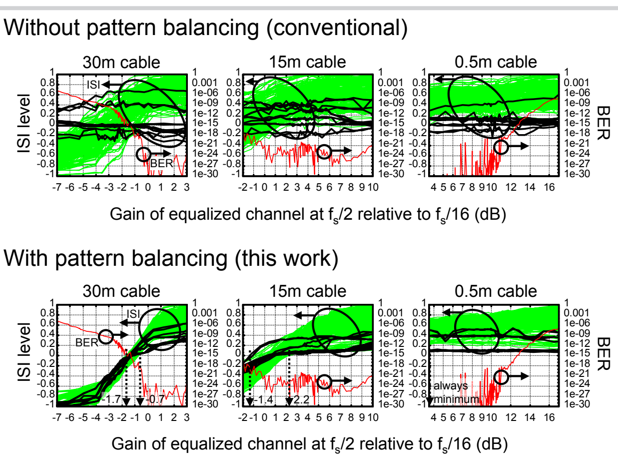
Filter Pattern	D0	D1	D2	D3	D4	B3	ISI level	EQ gain
FP0	L	L	L	L	H	L	-1 (under)	up
						H	+1 (over)	down
FP1	L	L	L	H	L	L	-1 (under)	up
						H	+1 (over)	down
FP2	H	H	H	L	H	L	+1 (over)	down
						H	-1 (under)	up
FP3	H	H	H	H	L	L	+1 (over)	down
						H	-1 (under)	up

b) Random-phase down sampling



- One sample per 32b (3G mode) or 64b (10G mode) is used to save power.
- Sampling phase is randomly changed to improve tolerance for middle-frequency jitter and periodic patterns that may be synchronous to the down-sampling cycle

Figure 24.4.4: Adaptive equalizer control scheme.



Notes)
1. ISI level is measured for 8B10B-encoded Ethernet frames filled with a fixed data byte. Highlighted solid lines are results for pathological data patterns which contain only low or high frequency component in the data payload.
2. BER is for PRBS31 and measured for >10^{-12} or estimated from measured bathtub curve.
3. Measured in 3G mode using AWG24 cables with TX pre-emphasis used in 10GBASE-CX4.

Figure 24.4.5: Evaluation results for the pattern tolerance.

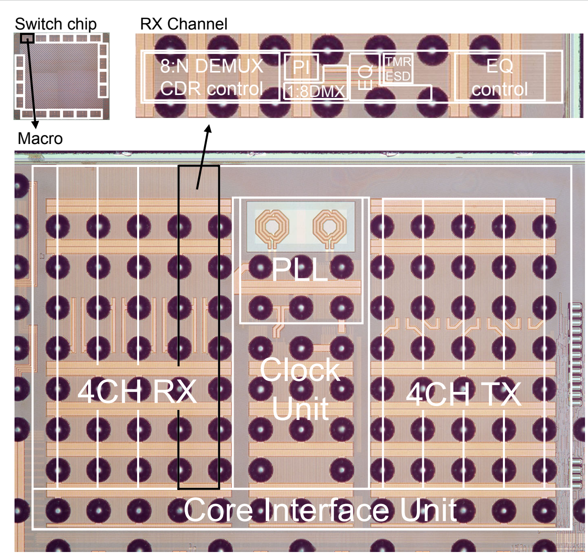


Figure 24.4.6: Chip and macro micrographs.

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